NASA Technical Memorandum 100426

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Abstract

Since 1982, the Western Aeronautical Test Range (WATR) of the Ames-Dryden Flight Research Facility has been separating the data acquisition and processing function required on all telemetry pulse code modulation (PCM) data and the display processing function required in the flight research mission control centers (MCCs). These two functions historically have been done on the same set of super-minicomputers remote from the MCCs. Removing the display processing function from the realm of the super-minis or telemetry-radar acquisition and processing system (TRAPS) and out into the MCCs will allow the research engineers the flexibility to configure their own display processing system to optimize performance during a flight research mission. Meanwhile, the TRAPS will have more time to acquire data. One of the processors chosen to handle the display processing function is an IBM PC/AT compatible rack-mounted personal computer. This class and type machine will not only allow the transfer of the display processing function into the MCCs, but also allow the research engineers a personalized set of analytic and display tools for use on their own unique sets of data. These tools can be purchased easily or developed in a short time, drawing from a wealth of off-the-shelf PC/AT compatible engineering hardware and software items. The integration of PC/AT machines into the MCC environment will help short-term goals as well as long-range plans develop in harmony in the WATR MCCs.

Nomenclature

ADC	analog to digital converter
ANCRT	alphanumeric CRT (cathode ray tube)
CAP	color alphanumeric panel
CGA	color graphics adapter
CRT	cathode ray tube
DAC	digital to analog converter
DSP	digital signal processing
EGA	enhanced graphics adapter
FTP	File Transfer Protocol
GWBASIC	Microsoft's BASIC language interpreter
IRIS	interactive raster imaging system
MAGIC	master graphics interactive console
MCC	mission control center
MDA	monochrome display adapter
MDB	memory mapped output board
PC	personal computer
PCM	pulse code modulation
RAM	random access memory
RBG	red, blue, green
RIG	real-time interactive graphics
RIM	real-time interactive map
SPIN	spin display
TCP/IP	Transmission Control Protocol/ Internet Protocol
TRAPS	telemetry-radar acquisition and processing system
TTL RGB	transistor/transistor logic — red, green, blue (a type of video standard)
WATR	Western Aeronautical Test Range

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Introduction

Within the Western Aeronautical Test Range (WATR), we use IBM PC (IBM, IBM PC, PC/XT/AT, and PS/2 Model 80 are trademarks of the International Business Machines Corporation)† compatible computers for our secretarial work (such as managerial and technical report generation) as well as for remote terminals to our super-minicomputer-based development telemetry system. In the past 5 years, the IBM PC and various compatible computers have evolved technically to meet the increasing computational demands. At present, the latest version of an IBM PC/AT computer, both hardware and software compatible, runs application programs 12 to 16 times as fast as the first IBM PC. With special hardware available off the shelf, this figure can be multiplied by 10 to 20 for some math routines. This is the class of machine that the WATR will be integrating into its mission control centers (MCCs). This machine, and its place within the MCCs and the telemetry-radar acquisition and processing system (TRAPS), is presented in detail. Before this, however, a system overview of the TRAPS and MCCs is in order.

†Use of trade names or names of manufacturers in this paper does not constitute an official endorsement of such products or manufacturers, either expressed or implied, by the National Aeronautics and Space Administration.

System Overview of the Telemetry-Radar Acquisition and Processing System and Mission Control Centers

Figures 1 and 2 present an overview of the WATR of the NASA Ames Research Center. In Fig. 1, the three main sites of the WATR are shown: Moffett Field, Crows Landing, and Dryden. Figure 2 depicts some of the many research aircraft flown out of the Dryden Flight Research Facility as well as some of the Dryden ground telemetry facilities. Figure 3 is a simplified pictorial block diagram of the various systems of the WATR that reside at the Ames-Dryden Flight Research Facility at Edwards, California. It shows the flow of data from the research aircraft down through the ground telemetry, space positioning, and communication facilities, then on to the TRAPS and MCCs. Figure 4 is a simplified block diagram of the two systems previously mentioned: the TRAPS and the MCCs. As already stated, the TRAPS at present handles not only the acquisition and processing function on all the telemetry pulse code modulation (PCM) and radar data, but the display processing function for the MCCs as well. As shown in Fig. 4, there are actually three TRAPS (designated nos. 1, 2, and 3) and two MCCs (designated the blue and gold mission control centers after their individual room colors). It is a continuing resolution within the WATR to evolve the three TRAPS and the two MCCs as identical systems. It has been resolved also that any one of the three TRAPS be able to drive or supply data to either of the two MCCs. To date, the WATR has been functionally successful in both these areas.

The Mission Control Center Display Processor Requirements

To begin a discussion of requirements for an MCC display processor, we first need to cover the various types of data and kinds of data displays used or foreseen in the MCCs.

At present each MCC (both the gold and blue rooms) has associated with it eight engineering consoles of three 19-in. racks each, a WATR range officer console, a bank of video monitors across one ceiling edge, and two large-screen high-resolution monitors (6 ft diagonally). Some of the consoles are being replaced with taller ones the second or third quarter of 1988 to allow the addition of the PC/AT display processors into the MCCs. Figures 5 and 6 show the blue and gold rooms as they appear today. Figure 7 is a basic MCC floor plan depicting the layout of both the blue and gold rooms. The eight engineering consoles are the main interest in regards to the PC/AT display processor. Figure 8 shows a present-day engineering console. Figure 9 depicts an engineering console of perhaps 2 years from now. The areas marked IRIS (interactive raster imaging system; IRIS 3030 and 4D/70GT are trademarks of Silicon Graphics Incorporated) are 2-D/3-D graphics super-workstations for graphics work that the PC/ATs are not capable of.

There are twelve analog strip chart recorders with eight channels each in each MCC. Typically there are two strip charts in each engineering console, two of the consoles having no strip charts in them. At this time there is only one cathode ray tube (CRT) display (red-blue-green monitor) in each console. As Fig. 9 shows, however, a second and perhaps a third monitor is planned to support the PC/AT display processor(s). The present single monitor can display any one of up to eight different remotely generated display screens, depending on a video switching network remotely controlled at each console. The eight different display screens are as follows:

1. RIM (real-time interactive map). Displays terrain and related radar and PCM data. This display is set up and controlled interactively at the engineering console via a keyboard and mouse combination. The large screen monitors are typically used to display RIM for research aircraft and chase aircraft tracking purposes. This program at present runs in a local MCC processor.

2. SPIN (spin display). This is a special spin display used by the F-18 research group. It is an excellent example of what is possible by moving the display processing function into the MCCs and allowing an MCC local processor to handle the display. This allows new and different displays to be programmed and put into service in a short time. The spin display was created in a few days and installed without the need for a complete TRAPS checkout and verification and validation.

3. RIG (real-time interactive graphics). This is a multipurpose graphics display program that runs on the superminis of the TRAPS. It drives a graphics processor in the MCCs. This program is targeted to be removed out of the TRAPS and into a display processor in the MCCs by May 1988. The program scheduled to replace it is display number 4 (MAGIC).

4. MAGIC (master graphics interactive console). This program runs in a local MCC processor. It provides all of the same functions that RIG has and is easily expanded to include additional functions. At present, the WATR has one console running MAGIC. A second console will be used to replace RIG by May 1988.

5. ANCRT, page 1 of 2 (an alphanumeric CRT display). This program at present runs on the TRAPS and is a prime candidate to run on the PC/ATs in the mission control centers. A variety of page formats is possible, including fixed and scrolled quarter, half- and full-page displays.

6. ANCRT, page 2 of 2 (second page identical in function to page 1).

7. Color panel number 1 of 2. This program runs on the TRAPS and uses the same type of graphics processor as RIG. Using character graphics with a character resolution of 80 by 40, a variety of displays can be implemented with a little imagination.

8. Color panel number 2 of 2. Identical in function to color panel number 1.

Of these eight displays now used in the WATR MCCs, number 3 (RIG) will be removed. The RIM, SPIN, and MAGIC displays will run on the IRIS graphics super-workstations planned for each engineering console. The function of the ANCRTs and

color panels will be replaced by a single program called "color-alphanumeric panel" (CAP) that will run on the PC/ATs in each console. Figure 10 shows a variety of displays now possible in the MCCs.

The data that is required by the MCC display devices can be categorized in terms of parameter update rates required for each type of display; in turn, an understanding of these rates can help us to integrate the new PC/AT display processors into the MCCs. At present, there are only two different types of displays in the MCCs – the strip charts and the CRT display screens. The strip charts can require a data rate of up to the sample rate of the PCM system on-board the aircraft. At this time the analog strip charts are only good up to frequencies of 50 to 100 Hz, depending upon how much mechanical filtering of the data can be tolerated by the engineer viewing it in real time. The WATR is currently in the procurement stage of replacing these analog strip charts with digital input strip charts that can be used with data frequencies of beyond 1000 Hz, or as great as the sampling rate of the PCM systems used to date. The CRT screens are used to display a variety of data to the engineers in real time, from solid structures in motion, charts and graphs, to simple alphanumerics and discretes. Because this data is being viewed and interpreted by human beings, the required screen update rate is generally somewhere between one to ten times a second (usually one to two). There is a third data type to be considered also: ensemble data for digital signal processing (DSP) work. The requirement is not necessarily a raw data rate requirement. The periodicity of the data is of prime concern here. With the different data sampling points within the entire telemetry system (the TRAPS as well as the aircraft) being historically asynchronous, data to be analyzed using the more common DSP methods must be assembled carefully and passed as blocks of data to the computer doing the work. At present, this kind of work is done by applying the PCM data to a digital to analog converter (DAC), filtering it, and then resampling with an analog to digital converter (ADC) at a DSP workstation remote from the mission control centers (a rather cumbersome method). It is intended that this type of analysis be moved into the MCCs and handled in an entirely digital manner on a PC/AT display processor.

To handle all the different types of data and data display hardware requirements of the MCCs, the PC/AT display processors, as well as the other new display processors (that is, the IRIS graphics super-workstations), will have to be integrated into the TRAPS-MCC system with several different interfaces. One of these is presented in some detail, along with two others, in the section entitled The Data Interface.

As already discussed, the WATR is removing the display processing function from the TRAPS and placing it in the hands of the engineering team in the MCCs. At this point the two processors chosen by the WATR to handle this function are the IRISs and the PC/ATs. The IRISs are already handling the RIM, SPIN, and MAGIC displays. The PC/ATs initially will be required to handle a program called CAP (color alphanumeric panel will be discussed in the section titled DSPlay and CAP: Special Application Software) that will functionally replace the present ANCRT (1 and 2) and color panel (1 and 2) displays. With each of the eight engineering consoles having both an IRIS and at least one PC/AT class machine, the number and type of graphic-CRT displays possible is unlimited. Whether they are purchased off the shelve, as several DSP display programs can be, or written in-house in BASIC, FORTRAN, C, or Assembly, the display possibilities will give our flight research engineers the flexibility required in today's scientific world.

The Western Aeronautical Test Range PC/AT Compatible Hardware

This section contains both a listing and a discussion of each piece of hardware the WATR will use in its PC/AT compatible implementation. There are hundreds of different hardware and software items that can be integrated into an IBM PC/XT/AT compatible PC. The items listed here constitute a base or foundation configuration which can be expanded easily to meet an engineer's particular analytical or display needs. The WATR PC/AT compatible is shown in a development rack in Fig. 11.

1. IBM XT/AT compatible rack mountable ruggedized computer base unit, Texas Microsystems Incorporated (TMI), model number 2001A. This unit contains eight passive AT slots and two passive XT slots along with cooling fans, keyboard connector, disk-mounting hardware, and a 200-W power supply. Rack slides can be purchased as well.

2. IBM PC/AT compatible 10 MHz CPU card with an 80287-10 (10 MHz) numeric co-processor chip. TMI model numbers 8286-1MEG and 80287-10. This card uses one AT slot in the base unit and contains 1 megabyte of memory.

3. Dual floppy and dual hard AT compatible disk controller, Western Digital model number WD1003WA2.

4. Seagate ST251 half-height 40 megabyte hard drive with an average access time of 40 msec, self-parking, six heads, 820 cylinders, and a mean time between failure (MTBF) of 20,000 hr.

5. Panasonic model 455 half-height 360 kilobyte floppy disk drive.

6. Panasonic model 475 half-height 1.2 megabyte floppy disk drive.

7. AT compatible style 5060 keyboard.

8. XT/AT compatible EVEREX MAGIC I/O card with a parallel port (LPT1 or LPT2) and two RS-232C ports (COM1 and COM2).

9. IMSI mouse systems optimouse. Connects to one of the COM ports. It is supplied with software drivers.

10. Epson FX-286e dot matrix printer with 32,000 character buffer and an IBM printer cable.

11. PC/AT compatible, 12 MHz 32-bit floating point array processor with an MS-FORTRAN 4.0 compatible math library. Systolic Systems model

number PC-100. This card plugs into a single AT card slot. The PC-100 application software library includes real vector operations, complex vector operations, real and complex matrix operations, signal processing operations, and computer graphics operations. This hardware and software promises an easy to use, high-powered, general purpose computer at each engineering console. Installation of both the hardware and software of this subsystem takes only 30 minutes and is immediatel, usable via FORTRAN.

The last three items on the list constitute the video subsystem of the WATR PC/AT. It is capable of supporting any of the many video standards that might be used by various application software packages written to run on an IBM PC/XT/AT compatible machine. The three main video standards of interest are the monochrome display adapter (MDA), color graphics adapter (CGA), and enhanced graphics adapter (EGA). Most software is written for one of these standards; so the user must have the right adapter board and video monitor for the software. The EVA/480 video adapter and the NEC multisync monitor (NEC America, Inc., Melville, New York) is one of several combinations of PC circuit boards and monitors that will support all three (MDA, CGA, and EGA) and others. The sum of all the attributes of all three of these video adapters can be thought of as a fourth video standard. It is the intent of the WATR to look at using the text mode graphics common to all three standards and the TTL 64 color standard of the EGA in implementing the color alphanumeric panel (CAP) application software that will be covered in the section DSPlay and CAP: Special Application Software.

The standard number of colors that can be displayed at any one time is 16 (numbers 0 through numbers 15). However, with EGA, any one of a palette of 64 colors to color numbers 0 through 15 can be assigned. The basic 16-color palette is made up from the three red, blue, and green (RBG) color signals and an intensity bit (I). Figure 12 shows the relationship among these transistor/transistor logic (TTL) signals (on/off) and the color that is produced. More signals are required (and a monitor that will accept and use them) to generate a palette of 64 colors. The 64-color palette is built from the three basic TTL color signals red, blue, and green with the addition of three more; these are the secondary red, blue, and green TTL signals as shown in Fig. 13. These signals allow four different intensity levels for each of the three RBG colors (00, 01, 10, and 11) for a total of 64 possible colors. Figure 14 is a listing of a GWBASIC (Microsoft, MS-DOS, MS-FORTRAN, MS-C, GWBASIC, and MS-QuickBASIC are trademarks of Microsoft Incorporated) program that will display all 64 colors in stages.

Figure 15 shows the valid text screen modes using the EVA/480 card (or circuit board) and the NEC multisync monitor. The WATR is contemplating using either the color 80 by 25 (2000 characters) or the color 80 by 43 (3440 characters) mode. Figure 16 is a listing of a GWBASIC program that will display all possible IBM PC standard ASCII characters, with all possible attributes on the screen. It first asks if the blinking attribute is to be demonstrated (it may irritate the eyes), and then asks for the text screen mode for the PC. We now need to discuss screen memory, characters, and their attributes.

Writing ASCII characters (alphanumeric or graphic) is a simple matter of writing ASCII code to the PC memory. Figure 17 is a representation of the text mode memory map. For example, to write an "A" in the lower right-hand corner of the screen in 80 by 25 color text mode, write &H41 (hex) or 65 (decimal) to location B800:0F9E (segment:offset). Again, as an example, to set the color of this character, its background color, and if it is to blink or not (its attributes), one would write an attribute byte (based on Fig. 18) to location B800:0F9F. Building graphics displays in this manner is referred to as text mode graphics and can generate meaningful displays in a straightforward manner.

12. NEC multisync monitor with cable, NEC model number JC-1401P3A. This TTL RGB color monitor is capable of synchronizing to all the IBM PC/XT/AT video standards. The most important of these are MDA, CGA, EGA, and enhanced EGA. A monitor of this capability is necessary to ensure hardware compatibility to all the various application software packages available on the market.

13. Tseng Labs EVA/480 video board with CMII option. This board is compatible with the MDA, CGA, EGA, and enhanced EGA video standards and supplies TTL RGB video to the monitor.

14. TTL RGB to analog RGB converter with EGA cable. MDA, CGA, EGA, and enhanced EGA compatible. COVID model 460 with options 1 and 2.

The Western Aeronautical Test Range PC/AT Compatible System Software

Four software packages available from Microsoft Corporation, Bellevue, Washington, are listed in this section. The BASIC programs listed in the last section were written in GWBASIC. These packages set the standards for the IBM PC/XT/AT compatible machines on the market today. Both the MS-FORTRAN and the MS-C compilers are tested engineering languages. The WATR also intends to review the QuickBASIC compiler, with its already established graphics commands and its link to subroutines in Assembly, as the language that CAP (covered in the next section) be written in. The four software packages are as follows: (1) MS-DOS 3.21 with GWBASIC; (2) MS-FORTRAN 4.0 compiler; (3) MS-C 5.0 compiler; (4) MS-QuickBASIC compiler.

DSPlay and CAP: Special Application Software

In this section, two application software packages that will be initially used on the WATR PC/AT MCC display processor are covered briefly. The first is the DSPlay (DSPlay is a trademark of the Burr-Brown Corporation) software. It is a digital signal processing (DSP) package available from the Burr-Brown Corporation, Tucson, Arizona. The second package, called color alphanumeric panel (CAP), is being written in-house at the Ames/Dryden Facility at the time of this writing.

The DSPlay software implements DSP algorithms in FlowGrams and SubGrams through flow-chart type

programming. Flowgrams and Subgrams correspond, respectively, to main programs and subroutines in more conventional programming terms. Figures 19, 20, and 21 show a Flowgram and its corresponding parameter listing, along with a typical display generated by DSPlay. The Flowgram is a block diagram which details the flow of signals through a DSP process. To assemble a Flowgram on the screen, the engineer chooses from a selection of functions and places these functions, via editing commands, into the individual blocks. While editing, the user determines the parameters of each function block, and draws the required interconnecting lines. By placing the cursor over any individual block, while in the block mode, and pressing *ENTER* the engineer can view, print, and edit the parameters for that block, pressing *ESC* when finished viewing and editing. This also works for viewing, printing, and editing the parameters unique to the entire Flowgram while in the Flowgram mode. Each block represents a signal processing function, and the lines indicate the flow of the signal. A Flowgram can have up to 30 blocks in it; however, an individual block can represent a SubGram, which in turn can have up to 30 function blocks. DSPlay takes data in a simple format of floating point numbers. It is easy to see the uses DSPlay could have in the WATR mission control center in a real-time environment.

The first job of the WATR PC/ATs will be to replace the ANCRT 1 and 2 displays and the color panel 1 and 2 displays by running a software package called CAP. With a PC/AT in each engineering console capable of running CAP when required, and the IRIS graphics machines running multiple copies of RIM, SPIN, and MAGIC as required, the complete present-day display processing function requirement will have been removed from the TRAPS and put into the MCCs. At this point the IRISs and PC/ATs can take on new tasks (such as DSPlay and general purpose FORTRAN programs).

CAP will be able to handle its job by running in the text color graphics mode described earlier. Both the ANCRT and color panel programs run in a similar mode. CAP will have to download setup information from the TRAPS and build its displays based on an 80 column by 40 row character matrix (using either alphanumeric or graphics characters with color attributes). These displays can be fixed or scrolling alphanumerics, bar graphs, and status panels. Figure 22 is a sketch of such a matrix (40 by 25). Examples of alphanumeric data and color panel type graphics in quarter-page formats are shown. Assuming CAP will allow up to eight full pages (80 by 40) of display (selectable one at a time by, perhaps, a screen menu and a mouse), and full-, half-, and quarter-page formats, either fixed or scrolling, then one PC/AT running CAP would have twice the display capability as all four present-day display screens.

The Data Interface

As mentioned earlier, integrating the two chosen MCC display processors will require the fabrication of several special data interfaces as well as making sure they are each equipped with standard computer to computer communication hardware and software. The WATR PC/AT will be equipped with RS-232C ports over which setup information and the like can be transmitted between it and the WATR TRAPS super-minis. It is planned as well to equip the WATR PC/AT with a standard Ethernet interface using the Transmission Control Protocol/Internet Protocol (TCP/IP) and File Transfer Protocol (FTP) standards. The special data interfaces required for this integration task are another matter. The WATR has chosen to design and build these interfaces in-house at the Ames-Dryden Facility. Their conceptional design is such that after the first two designs are implemented, the system can be operational. As each new design is completed and installed, the system is enhanced and therefore will evolve with time. In this way, the WATR will not be overburdened with a dozen designs all at once with the impossible task of making sure they all play simultaneously.

There are three special interface designs. Two of them form the data link between the TRAPS and the WATR PC/AT. Conceptionally they can be looked at as a single design. However, the two parts will be used in other areas as well and don't necessarily have to go together. The third is a shared memory scheme between two WATR PC/ATs.

The first two interfaces to be designed are the memory mapped output board (MOB) and the PC/AT 2-port RAM (Fig. 23). The MOB is basically a parallel to serial converter and transmitter that resides on the Gould SEL-bus of the TRAPS (Gould Computer Systems Division, Fort Lauderdale, Florida). The MOB takes parallel data off the SEL-bus, it is then simultaneously written to the computer's memory. A FIFO (first in – first out) is used to buffer this data while the conversion to serial takes place and the data stream, with sync, is sent out. This stream is then sent to a 1 to 12 splitter and the 12 identical streams are, or can be, fed to as many as 12 PC/AT 2-port RAMs. The 2-port RAMs then sync up to the stream, do a serial to parallel conversion on the data, and write it into memory via the external port on the PC/AT bus. This link works in a broadcast mode, with data only flowing one way. Any protocol between the TRAPS and the PC/AT would have to be communicated via an Ethernet or RS-232C link. This link allows data to be merely written into the TRAPS memory to have it appear in the PC/AT memory as well. This process is totally transparent to the system software and the engineer using the PC/AT.

The third special interface is presented here in more detail. Figure 24, sheets 1 and 2, is a conceptual schematic of this interface and includes a short discussion of its operation. This design is intended to show a possible way of communication between two WATR PC/ATs. With it the two PC/ATs (or XTs) share a small 2 kilobyte area of memory. There is no interference and no delay in communication. It can make the two PC/ATs a two-processor machine with the right attention shown to application software packages.

Summary: Future Mission Control Centers

It is important to the WATR development effort that we maintain as few different pieces of equipment as possible in the MCCs. This is especially true when it comes to the computers to be used as

display processors. Each different computer means a different set of hardware and system software to learn, program, and maintain. The WATR had to choose systems with a good promise of evolving technology — from the microprocessors used, to the system and bus architectures, up to the newest in system software, all with an eye to keeping as much downward and upward compatibility as possible. Software is expensive to develop as well as to maintain, and generally all is lost when a new incompatible computer system is introduced. The IBM PC machine has grown from a relatively simple 8-bit personal computer with monochrome graphics to a 32-bit multi-user computer (that is, the micro channel-based IBM PS/2 Model 80) with high resolution color graphics. Software developers offer their application software packages upgraded for each new level of machine, and the programs that run on that first PC also run on the latest, given careful integration. For the WATR engineers, the key was to choose systems each year that would be of a different generation yet maintain software compatibility, not just new totally different systems. The WATR chose two systems that can handle the MCC display processing function for the next several years.

The future MCC should contain three or four generations of the IBM PC compatible; and they should all be capable of running the latest version of CAP and DSPlay as well as high-performance software on the high-performance (and latest) PC hardware.

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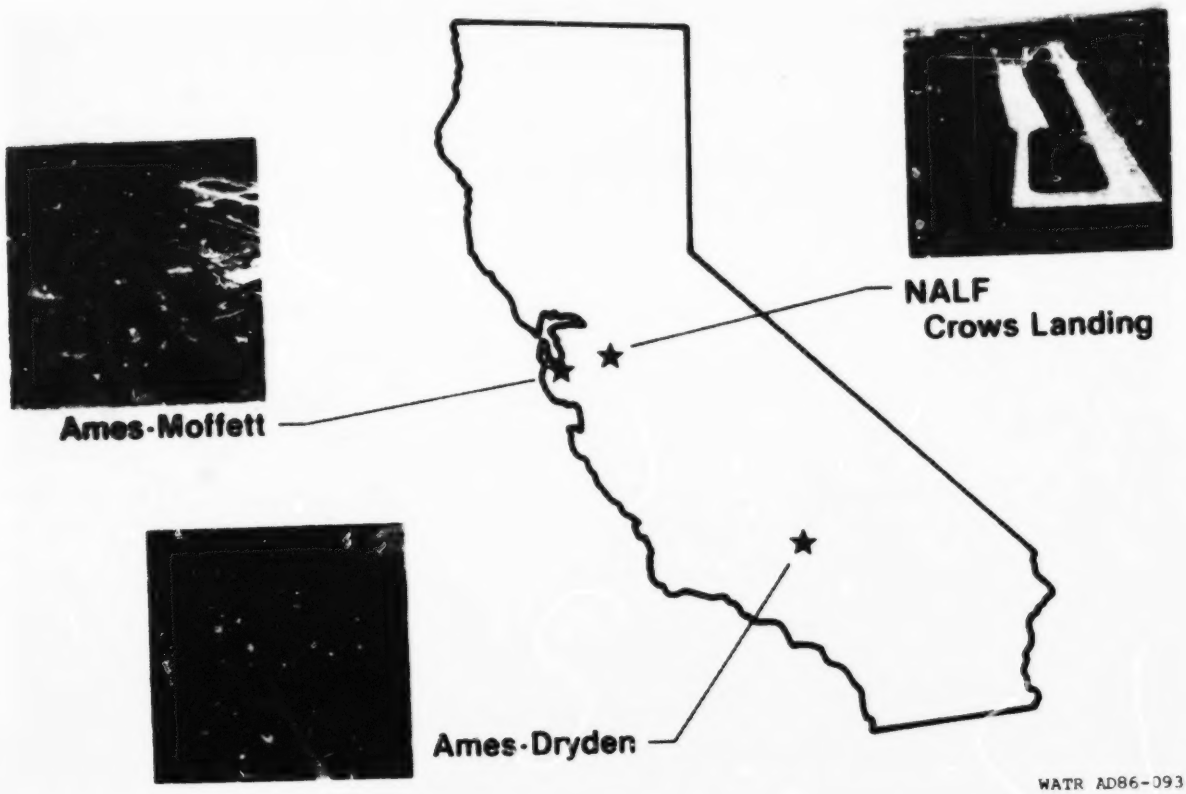

Fig. 1 Western Aeronautical Test Range, NASA Ames Research Center.

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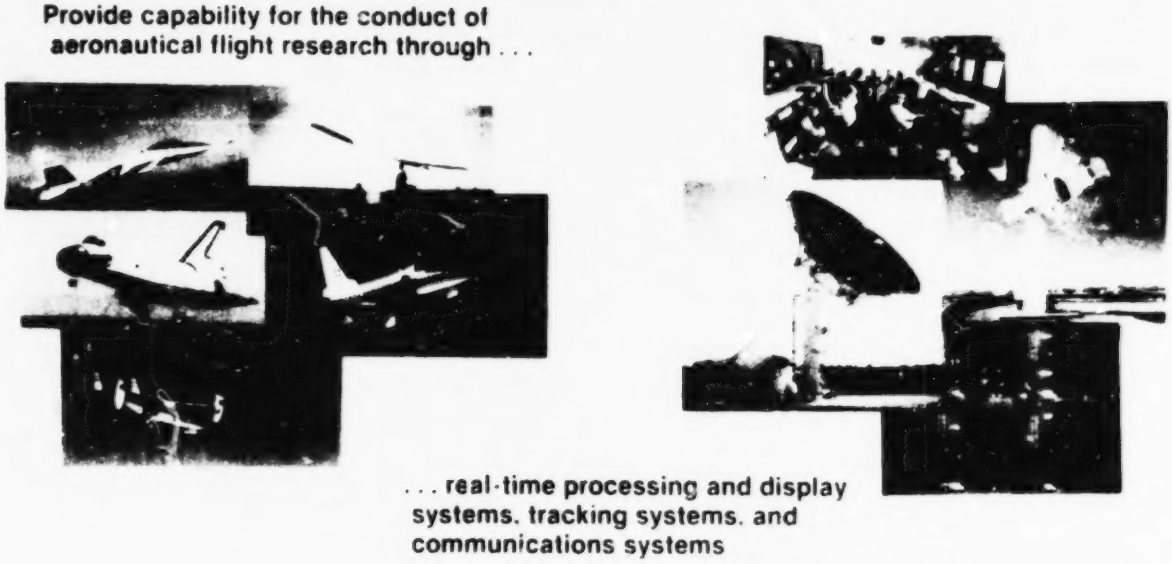
Provide capability for the conduct of aeronautical flight research through . . .
. . . real-time processing and display systems, tracking systems, and communications systems
WATR AD85-965

Fig. 2 Mission of Western Aeronautical Test Range.

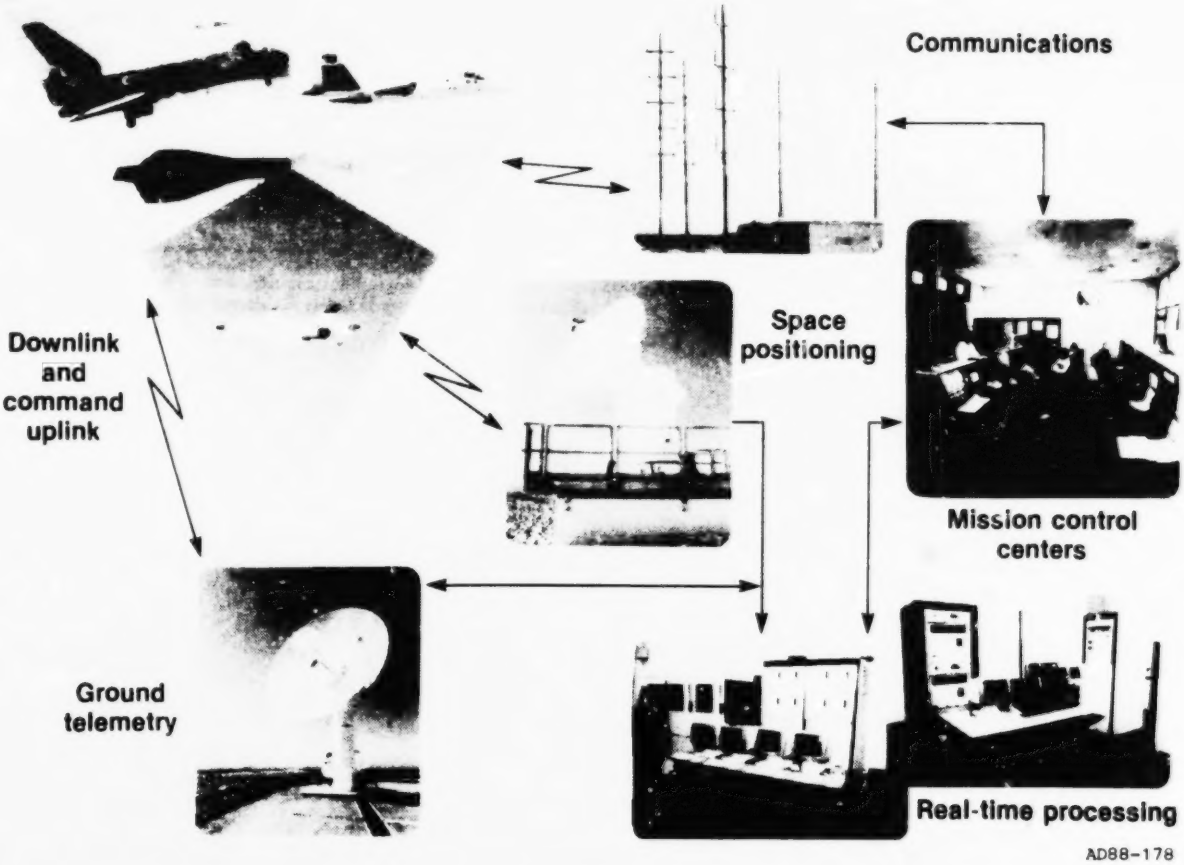

Fig. 3 Western Aeronautical Test Range systems at Dryden Flight Test Facility.

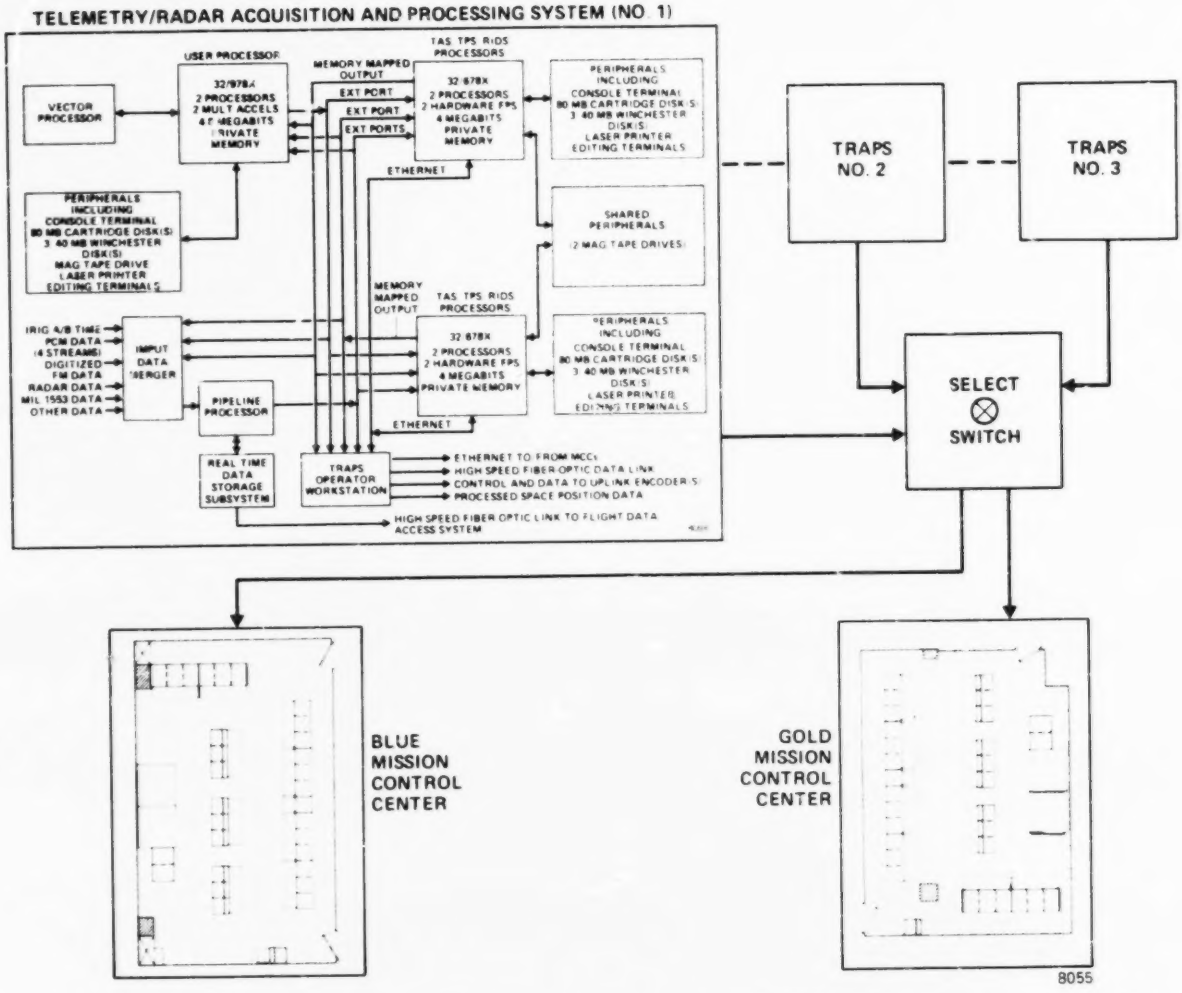

Fig. 4 Block diagram of three telemetry – radar acquisition and processing systems and two mission control centers.

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Fig. 5 Blue room, mission control center.

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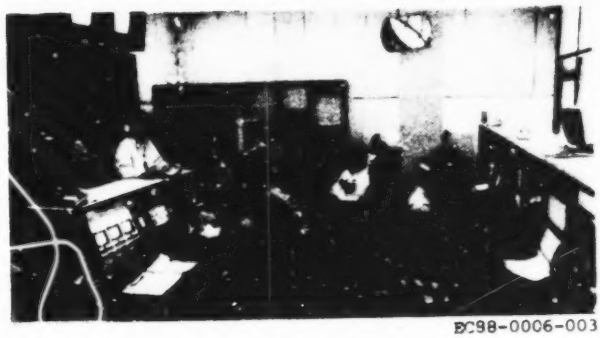

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Fig. 6 Gold room, mission control center.

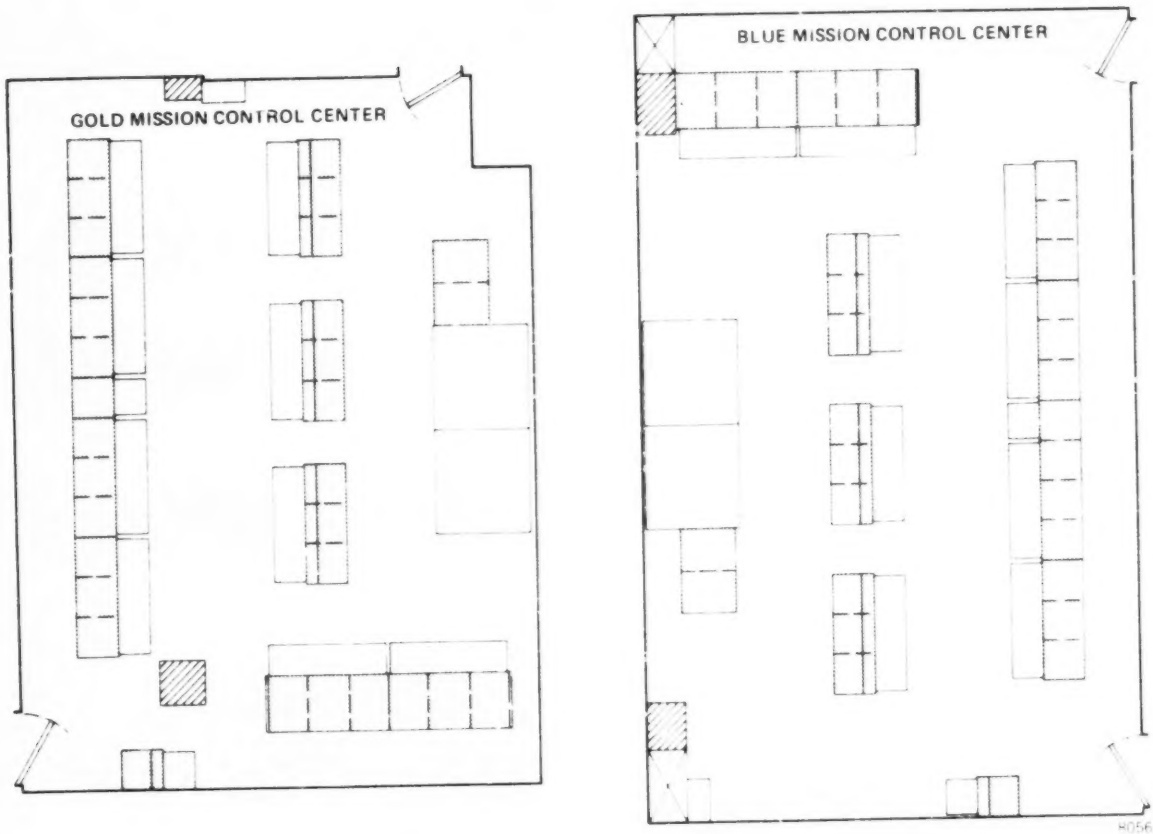
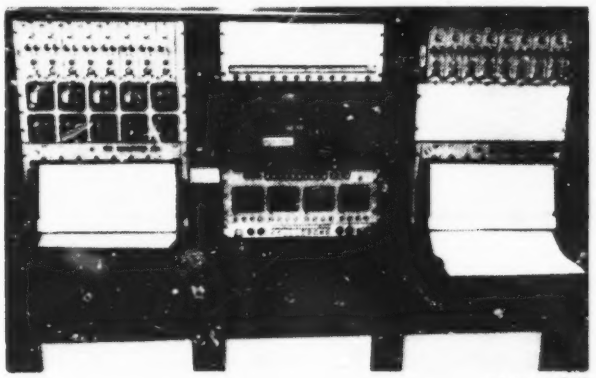


Fig. 7 Basic floor plan of mission control center.



ECN-31789

Fig. 8 Engineering console.

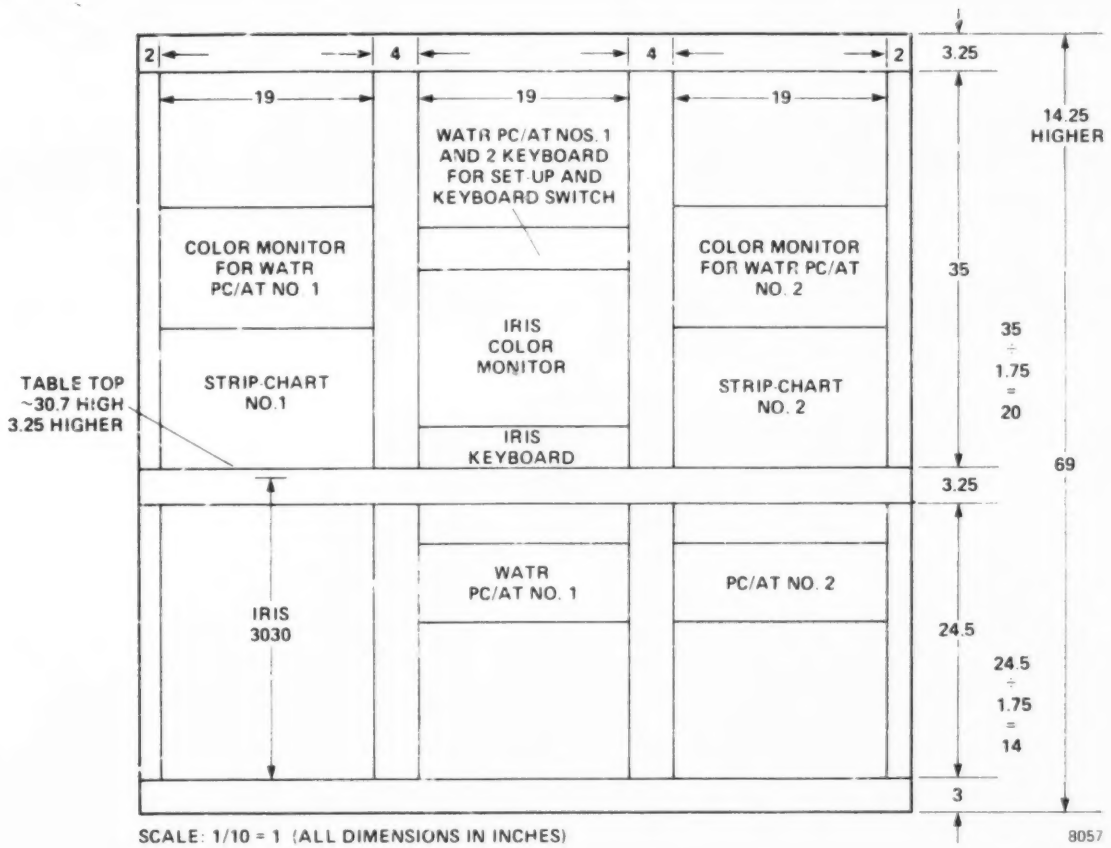


Fig. 9 Sketch of future engineering console.

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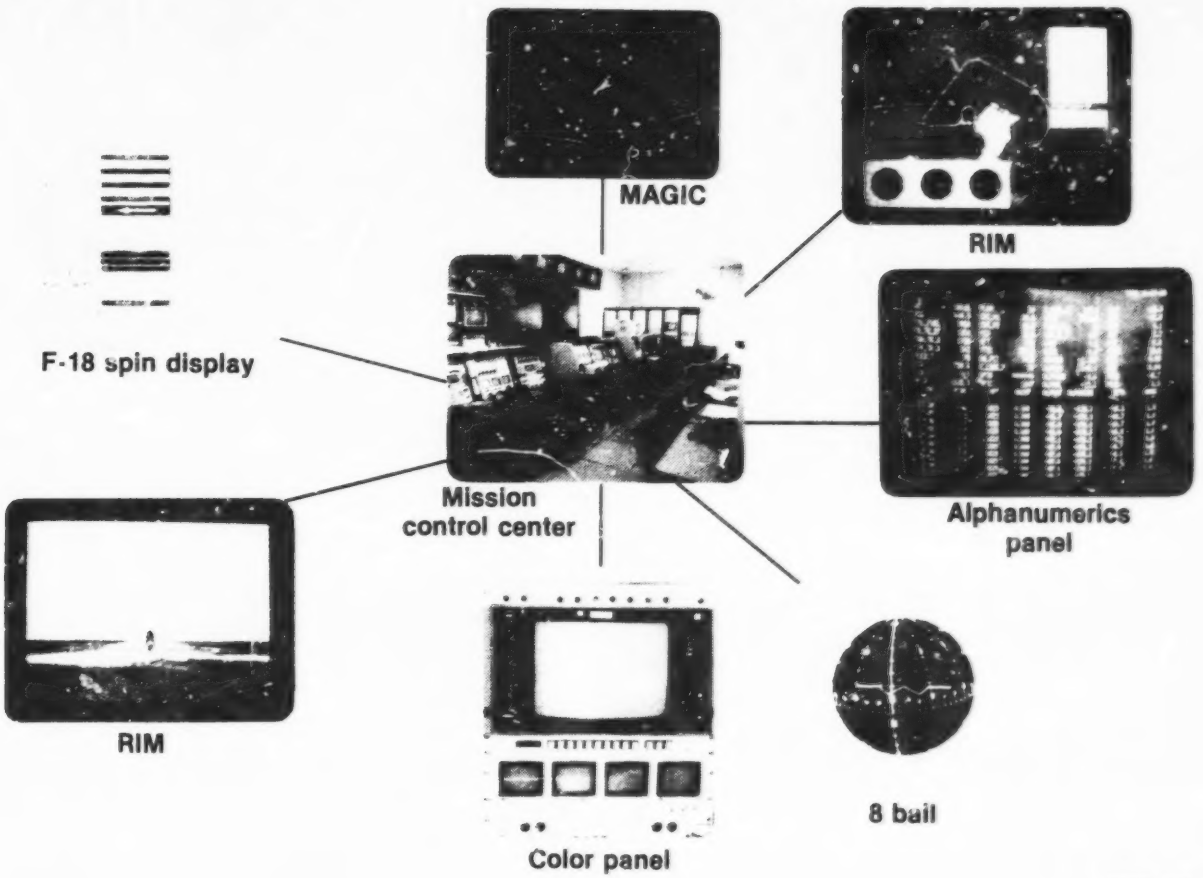
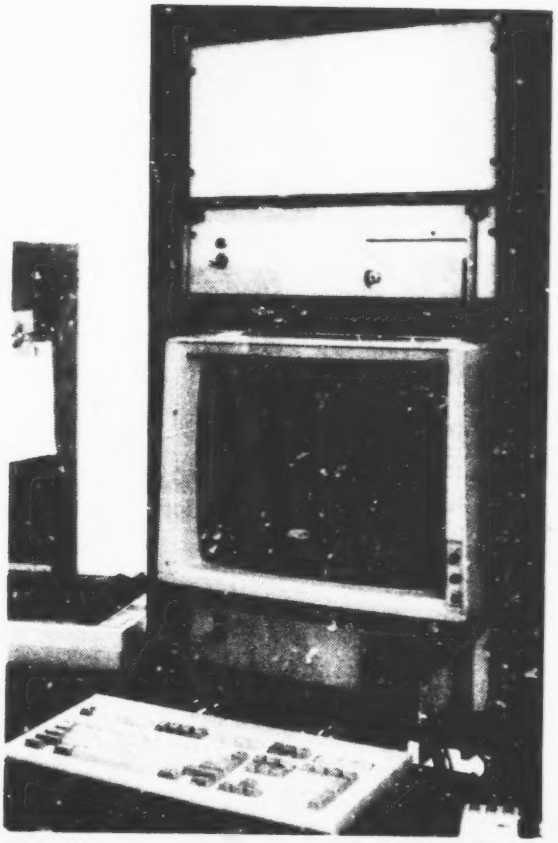


Fig. 10 Variety of data displays in mission control center.



EC88-0006-002

Fig. 11 PC/AT development at Western Aeronautical Test Range.

IRGB*	No.	Color
0000	0	Black
0001	1	Blue
0010	2	Green
0011	3	Cyan (blue-green)
0100	4	Red
0101	5	Magenta
0110	6	Brown (or dark yellow)
0111	7	Light grey (or ordinary white)
1000	8	Dark grey (black on many screens)
1001	9	Light blue
1010	10	Light green
1011	11	Light cyan
1100	12	Light red
1101	13	Light magenta
1110	14	Yellow (or light yellow)
1111	15	Bright white

*I = intensity, R = red, G = green, B = blue.

8059

Fig. 12 Basic 16-color palette.

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Direct drive video
display connector

Signal name — description	Pin
Ground	1
Secondary red	2
Primary red	3
Primary green	4
Primary blue	5
Secondary green/intensity	6
Secondary blue/mono video	7
Horizontal retrace	8
Vertical retrace	9

8060

Fig. 13 Video display adapter output connector for transistor/transistor logic — red, green, blue.

```
 10  SCREEN 9
 20  A=0
 30  DELAY=0
 40  B=A+48
 50  C=0
 60  CLS
 70  X=0
 80  Y=0
 90  XAXIS=2
100  YAXIS=10
110  FOR K=A TO B STEP 16
120  PALETTE C,K
130  LINE (X,Y)-(X+150,Y+150),C,BF
140  C=C+1
150  X=X+160
160  LOCATE YAXIS, XAXIS
170  XAXIS=XAXIS+20
180  PRINT "COLOR #"K
190  NEXT K
200  DELAY=DELAY+1
210  IF DELAY<1000 GOTO 200
220  A=A+1
230  IF A<16 GOTO 30
240  PALETTE
250  CLS
260  END
```

8061

Fig. 14 BASIC program color test.

Valid selections (assuming the appropriate display adapters are installed) are as follows:

* 40×25 color text mode : CO40
* 80×25 color text mode : CO80
* 80×25 mono text mode : MONO
* 132×25 color text mode : CO132×25
* 132×28 color text mode : CO132×28
* 132×44 color text mode : CO132×44
* 80×43 color text mode : CO80×43
* 80×43 mono text mode : MO80×43
* 80×60 color text mode : CO80×60
* Mode 0,1,2,3,4,5,6,7,D,E,F,10, 22,23,24,26 : the corresponding mode number
* Force a monitor that supports both MONO and COLOR : GOMONO, GOCOLOR

or run EMODE with no selection to get a selection menu.

** Mode 26 (CO80×60) requires an NEC MultiSync monitor

8062

Fig. 15 Valid text modes using the EVA/480 and NEC multisync.

```
10 DEF SEG=&HB800
20 INPUT "ENTER &HFF FOR BLINKING OR &H7F FOR NO
     BLINKING";I
30 INPUT "ENTER &HF9F FOR 80X25, &H1A0F FOR
     80X43,&H205F FOR 132X44";E
40 C=&H0
50 D=&H0
60 A=&H0
70 FOR B=A TO E STEP 2
80 POKE B,D
90 POKE (B+1),C
100 C=C+1
110 D=D+1
120 IF C>I THEN C=0
130 IF D>&HFF THEN D=0
140 NEXT B
150 DEF SEG
160 END
```

8063

Fig. 16 BASIC program Textgraf.

EVEN ADDRESSES FOR ASCII ODD ADDRESSES FOR ATTRIBUTE
TWO BYTES FOR EACH CHARACTER ON THE SCREEN

C 1 > DEBUG < E>
-rds < E>
DSXXXX B800 < E>
-f0 F9F XX < E>
ATTRIBUTE
-Q TO QUIT < E>

0000	0002	0004	0006	0008	000A	0094	0096	0098	009A	009C	009E	158
0001	0003	0005	0007	0009	000B	0095	0097	0099	009B	009D	009F	159
00A0											013E	318
00A1											013F	319
0140											01DE	478
0141											01DF	479
01E0											027E	639
01E1											027F	639
0280											031E	799
0281											031F	799
0320											0BDF	3039
0BE0											0C7F	3199
0C80											0D1E	3358
0C81											0D1F	3359
0D20											0DBE	3518
0D21											0DBF	3519
0DC0											0E5E	3678
0DC1											0E5F	3679
0E60											0EFE	3838
0E61											0EFF	3839
0F00	0F02	0F04	0F06	0F08	0F0A	0F94	0F96	0F98	0F9A	0F9C	0F9E	3998
0F01	0F03	0F05	0F07	0F09	0F0B	0F95	0F97	0F99	0F9B	0F9D	0F9F	3999

960
1120
1280
1440
1600
1760
1920
2080
2240
2400
2560
2720
2880

$(800 \cdot 25) \cdot 2 = 4000_{10}$ BYTES

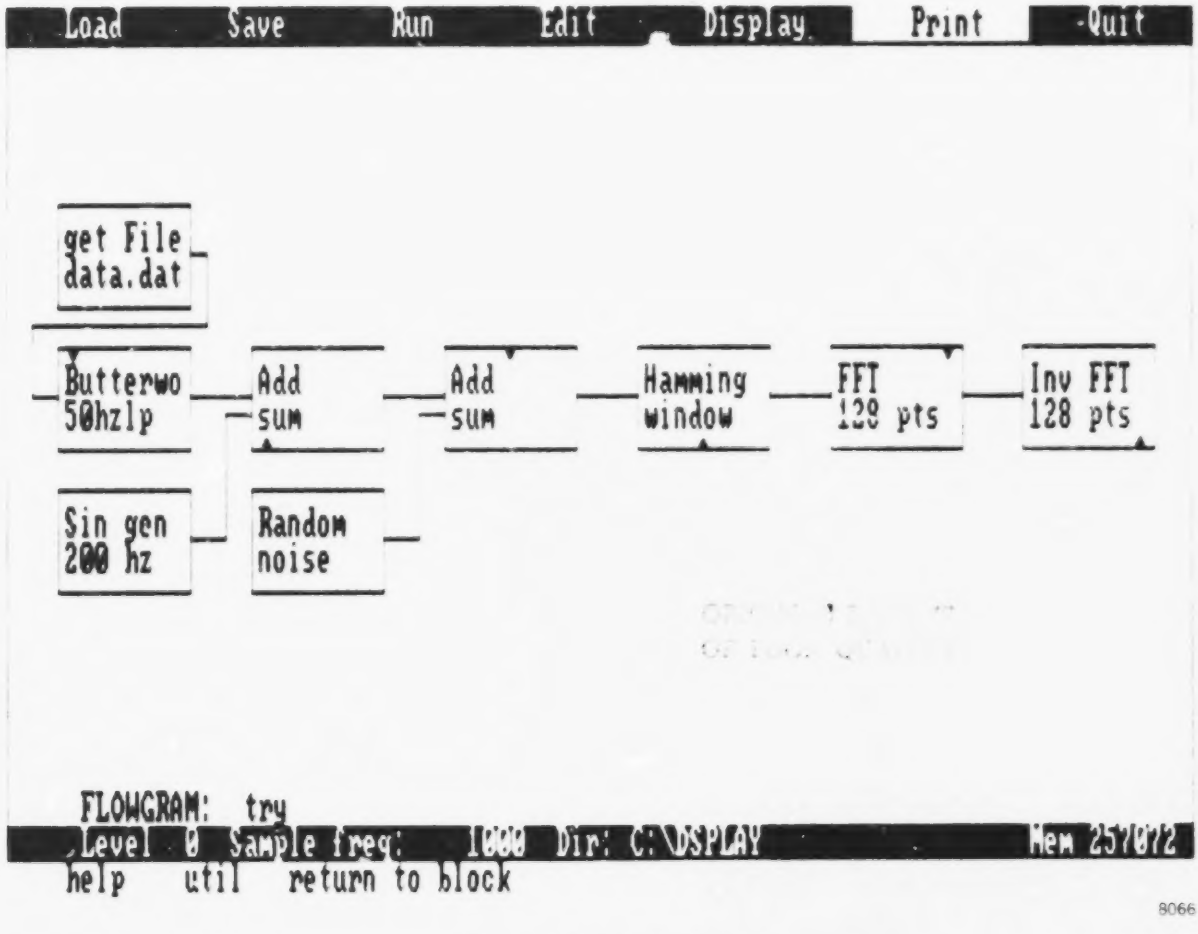
8065

Fig. 17 Test mode screen memory map.

1st nibble of attribute byte identifies 1 of 8 background colors AND if foreground is blinking or not.		2nd nibble of attribute byte identifies 1 of 16 foreground colors.	
Black	0	0	Black
Dark blue	1	1	Dark blue
Dark green	2	2	Dark green
Light blue (low intensity) (cyan)	3	3	Light blue (low intensity) (cyan)
Dark red	4	4	Dark red
(magenta) Dark purple	5	5	dark purple (magenta)
Dark brown	6	6	Dark brown
Grey	7	7	Grey
		8	Dark grey
Same 8 background color choices but foreground color blinks	8	9	Bright dark blue
	9	A	Light green
	A	B	Bright light blue (light cyan)
	B	C	Light red
	C	D	Light purple (light magenta)
	D	E	Light yellow
	E	F	Bright white
	F		

8064

Fig. 18 Character attributes.



8066

Fig. 19 DSPlay FlowGram.

```
Block Parameters:
    Block Name:  data.dat
    Function Type:  get File
        file Name:  data.dat
    output buffer lenyth:                128          data type <R,C>:   R
        input file offset:                0           frame overlap:     0

    Block Name:  50hzlp
    Function Type:  Butterwo
             sample frequency:                  1000
             cutoff frequency:                    50
             center frequency:                     0
          frequency bandwidth:                     0
          lo cutoff frequency:                     0
          hi cutoff frequency:                     0
               pass band gain:                     1
          pass band ripple(dB):                    0
    stop band attenuation(dB):                     0
      number of poles (to 20):                     6
    number of taps (3 to 256):                     0
    number of bands (1 to 10):                     0

    Block Name:  200 hz
    Function Type:  Sin gen
         frequency (hertz):          200
         amplitude (volts):            1
        phase shift (deg.):            0

    Block Name:  sum
    Function Type:  Add

    Block Name:  noise
    Function Type:  Random
        amplitude (volts):            1

    Block Name:  sum
    Function Type:  Add

    Block Name:  window
    Function Type:  Hamming

    Block Name:  128 pts
    Function Type:  FFT
        buffer length [16,32,..2048]          128

    Block Name:  128 pts
    Function Type:  Inv FFT
        buffer length [16,32,..2048]          128

                                                                        8067
```

Fig. 20 FlowGram parameter list.

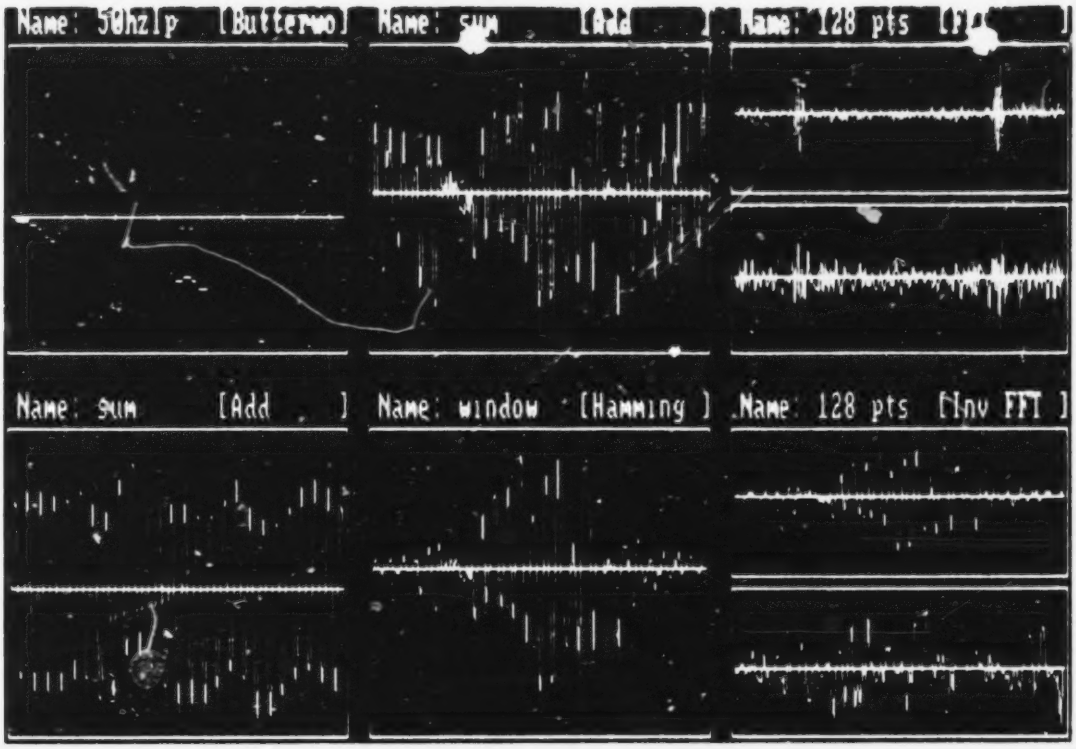

Name: 50hz lp [Butterwo
Name: sum [Add
Name: 128 pts [Inv FFT]
Name: sum [Add]
Name: window [Hamming]
Name: 128 pts [Inv FFT]
BAR press spacebar to continue
8068

Fig. 21 DSPlay graphs.

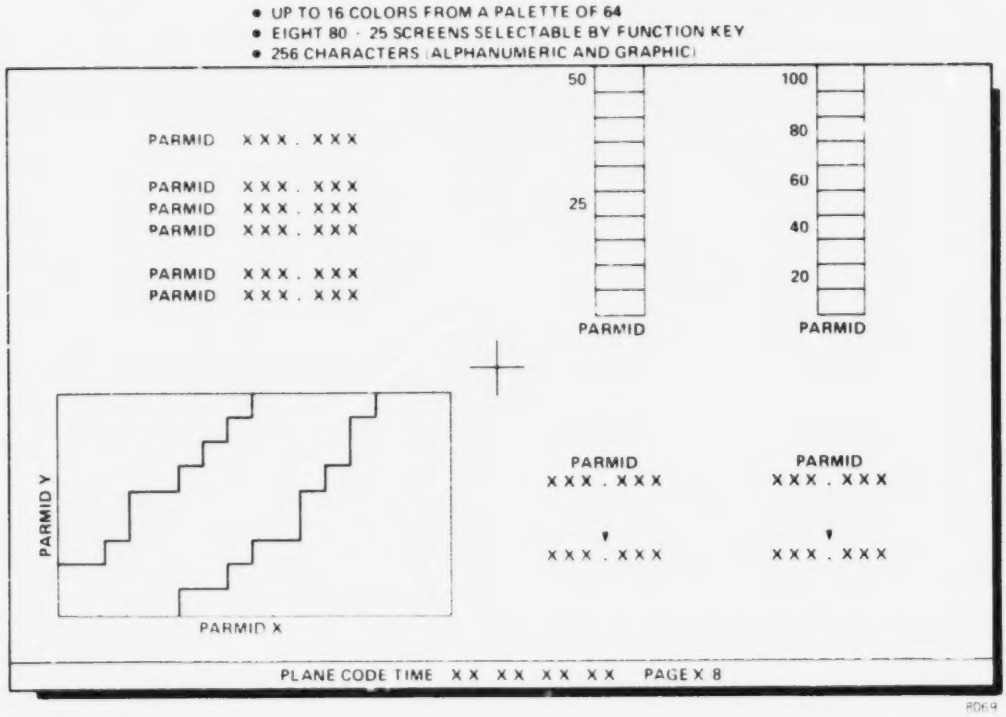


Fig. 22 Sketch of a 40 by 25 character CAP screen.

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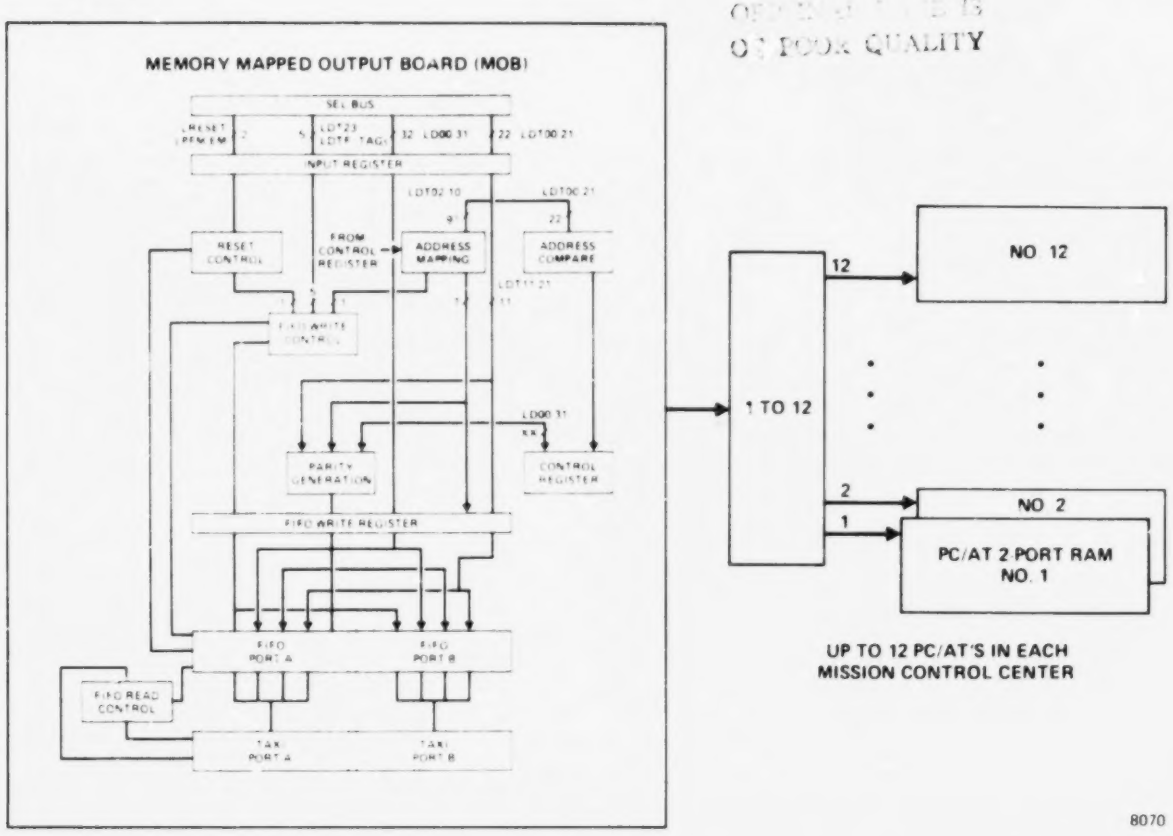

Fig. 23 Memory mapped output board and PC/AT 2-port random access memory.

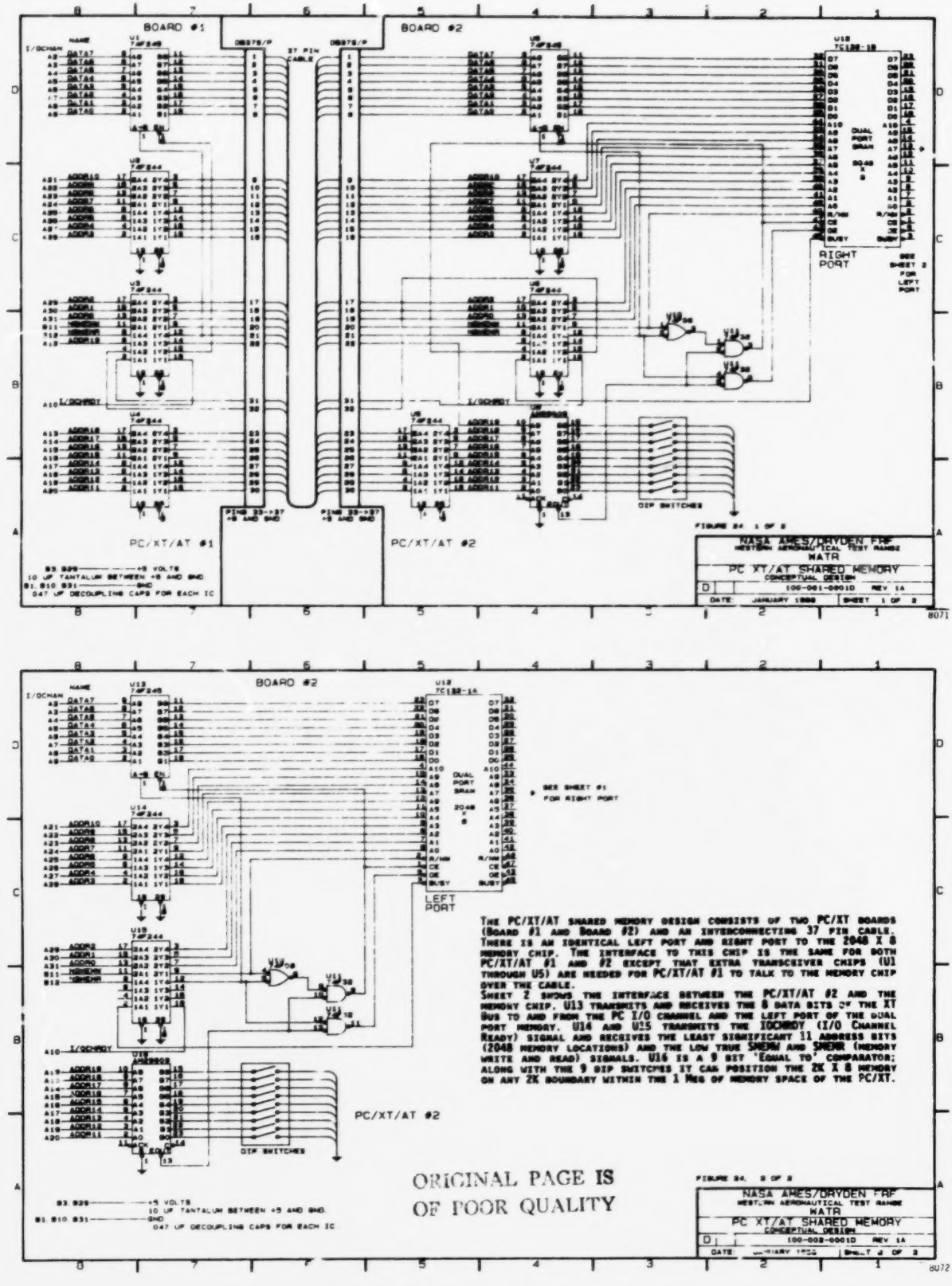
BOARD #1
BOARD #2
PC/XT/AT #1
PC/XT/AT #2
RIGHT PORT
LEFT PORT
DIP SWITCHES
NASA AMES/DRYDEN FRF
WATR
PC XT/AT SHARED MEMORY
CONCEPTUAL DESIGN
THE PC/XT/AT SHARED MEMORY DESIGN CONSISTS OF TWO PC/XT BOARDS (BOARD #1 AND BOARD #2) AND AN INTERCONNECTING 37 PIN CABLE. THERE IS AN IDENTICAL LEFT PORT AND RIGHT PORT TO THE 2048 X 8 MEMORY CHIP. THE INTERFACE TO THIS CHIP IS THE SAME FOR BOTH PC/XT/AT #1 AND #2 EXCEPT THAT EXTRA TRANSCEIVER CHIPS (U1 THROUGH U5) ARE NEEDED FOR PC/XT/AT #1 TO TALK TO THE MEMORY CHIP OVER THE CABLE.
SHEET 2 SHOWS THE INTERFACE BETWEEN THE PC/XT/AT #2 AND THE MEMORY CHIP. U13 TRANSMITS AND RECEIVES THE 8 DATA BITS OF THE XT BUS TO AND FROM THE PC I/O CHANNEL AND THE LEFT PORT OF THE DUAL PORT MEMORY. U14 AND U15 TRANSMITS THE IOCHRDY (I/O CHANNEL READY) SIGNAL AND RECEIVES THE LEAST SIGNIFICANT 11 ADDRESS BITS (2048 MEMORY LOCATIONS) AND THE LOW TRUE SMEMW AND SMEMR (MEMORY WRITE AND READ) SIGNALS. U16 IS A 9 BIT 'EQUAL TO' COMPARATOR; ALONG WITH THE 9 DIP SWITCHES IT CAN POSITION THE 2K X 8 MEMORY ON ANY 2K BOUNDARY WITHIN THE 1 MEG OF MEMORY SPACE OF THE PC/XT.
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Fig. 24 PC/AT shared memory design.

NASA National Aeronautics and Space Administration

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16. Abstract

Since 1982, the Western Aeronautical Test Range (WATR) of the Ames-Dryden Flight Research Facility has been separating the data acquisition and processing function required on all telemetry pulse code modulation (PCM) data and the display processing function required in the flight research mission control centers (MCCs). These two functions historically have been done on the same set of superminicomputers remote from the MCCs. Removing the display processing function from the realm of the superminis or telemetry-radar acquisition and processing system (TRAPS) and out into the MCCs will allow the research engineers the flexibility to configure their own display processing system to optimize performance during a flight research mission. Meanwhile, the TRAPS will have more time to acquire data. One of the processors chosen to handle the display processing function is an IBM PC/AT compatible rack-mounted personal computer. This class and type machine will not only allow the transfer of the display processing function into the MCCs, but also allow the research engineers a personalized set of analytic and display tools for use on their own unique sets of data.

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